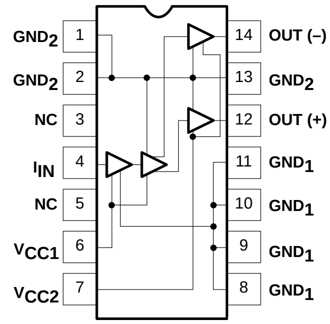
Transimpedance amplifier (280MHz) NE5210

DESCRIPTION

The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

PIN CONFIGURATION

D Package



TOP VIEW

SD00318

FEATURES

- Low noise: 3.5pA/√Hz
- Single 5V supply
- Large bandwidth: 280MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- High overload threshold current
- Wide dynamic range
- 7kΩ differential transresistance

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5210D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Operating junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Power dissipation, T_A=25°C (still air)[1]	1.0	W
I_{INMAX}	Maximum input current[2]	5	mA

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W.
2. The use of a pull-up resistor to V_{CC} for the PIN diode, is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±120	±160		µA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±160	±240		µA

NOTES:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

Typical data and Min/Max limits apply at V_{CC}=5V and T_A=25°C.

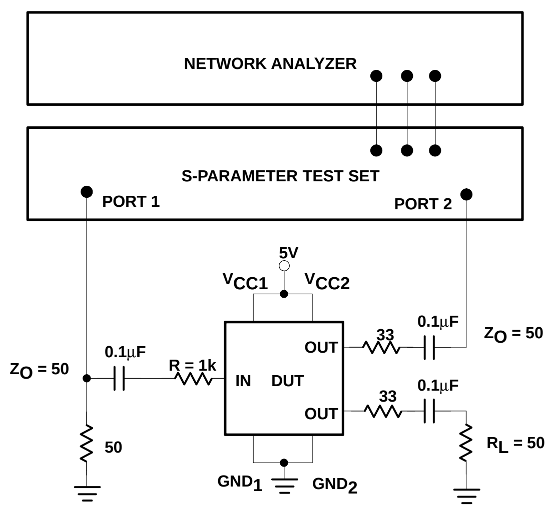
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L=\infty$ Test Circuit 8, Procedure 1	4.9	7	10	kΩ
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L=\infty$	2.45	3.5	5	kΩ
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1, T_A=25°C	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC}=5±0.5V		9.6	20	%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A=T_{A\,MAX}-T_{A\,MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	f=10MHz, T_A=25°C Test Circuit 2		3.5	6	pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S=0[1]	T_A=25°C Test Circuit 2 Δf=100MHz Δf=200MHz Δf=300MHz		 37 56 71		nA
	C_S=1pF	Δf=100MHz Δf=200MHz Δf=300MHz		40 66 89		
PSRR	Power supply rejection ratio[2] ($V_{CC1}=V_{CC2}$)	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	f=0.1MHz, Test Circuit 6		23		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OMAX}	Maximum output voltage swing differential	$R_L=\infty$ Test Circuit 8, Procedure 3	2.4	3.2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0.8	1.2	ns

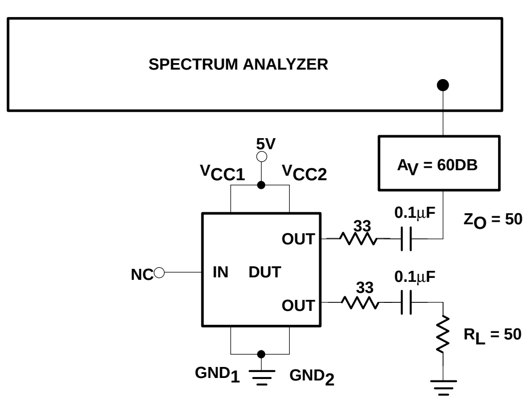
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by a -3dB bandwidth test.

TEST CIRCUITS



SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 33$	$R_O = 2Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 66$

Test Circuit 1



Test Circuit 2

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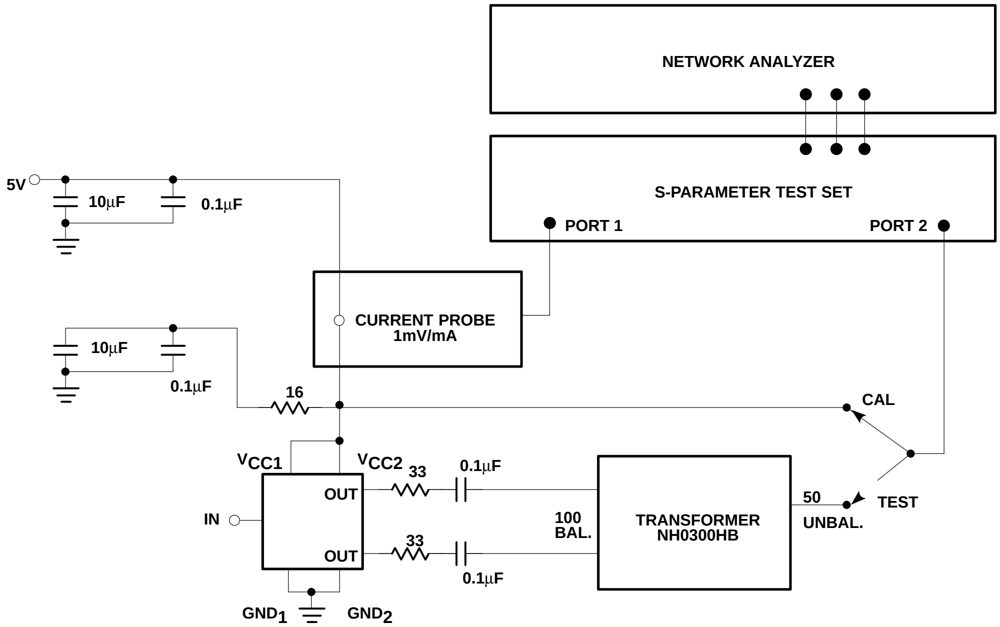
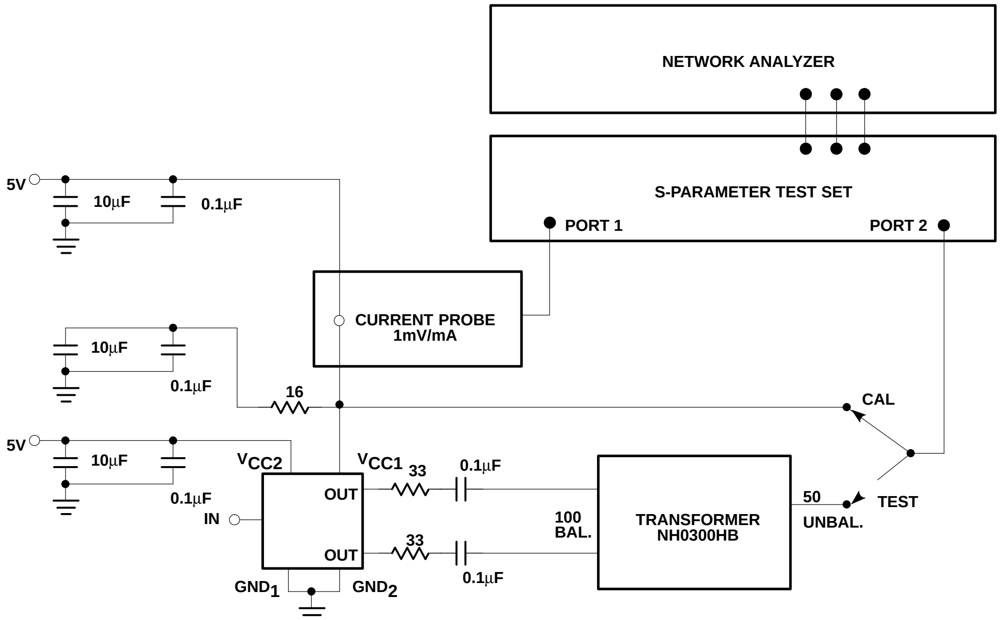
TEST CIRCUITS (Continued)



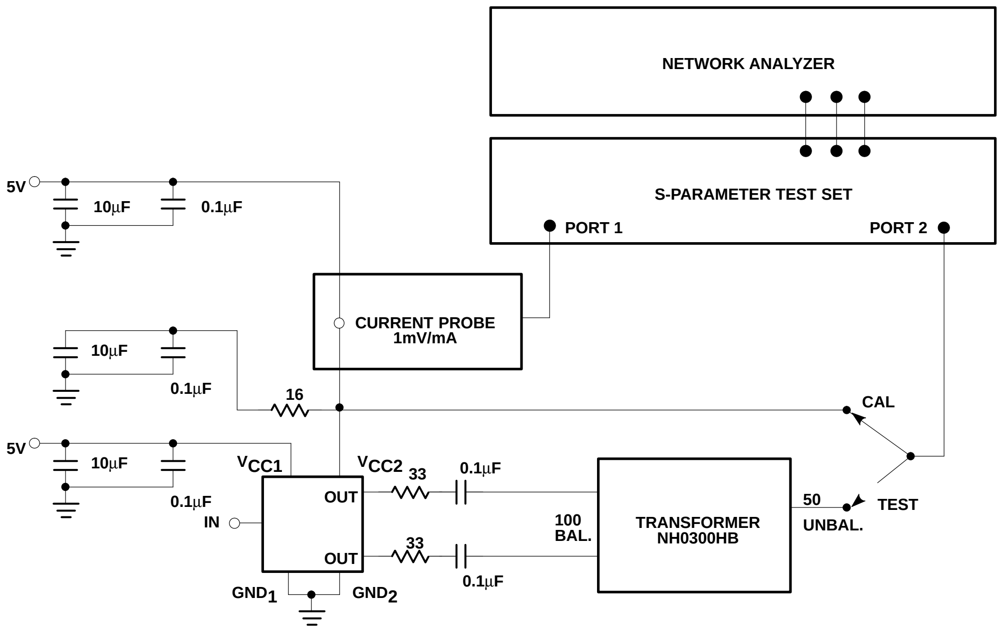
Test Circuit 3



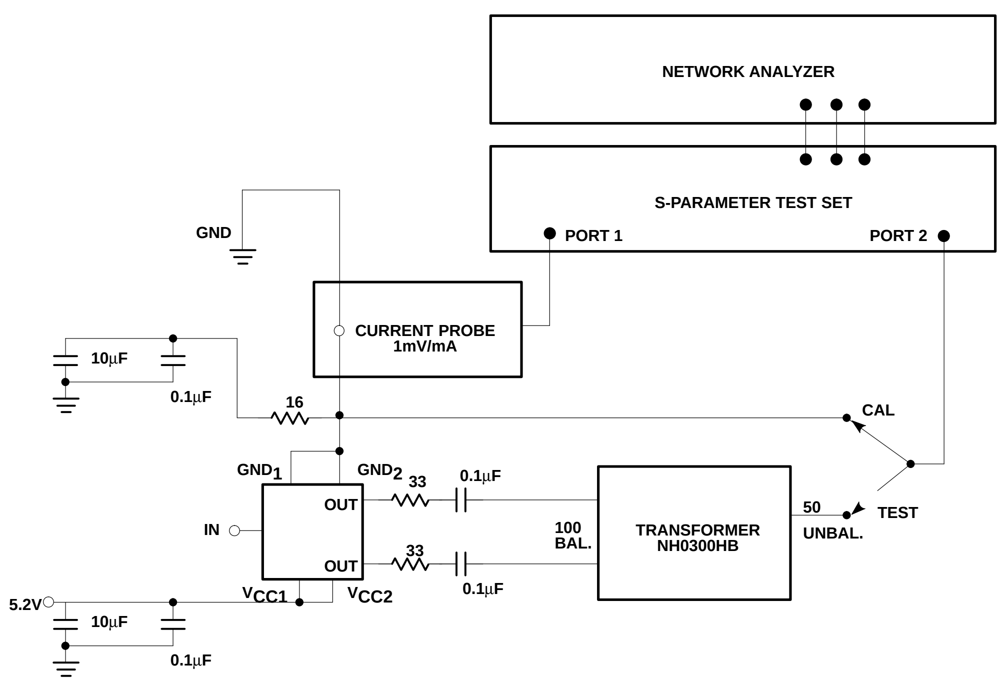
Test Circuit 4

SD00320

TEST CIRCUITS (Continued)



Test Circuit 5



Test Circuit 6

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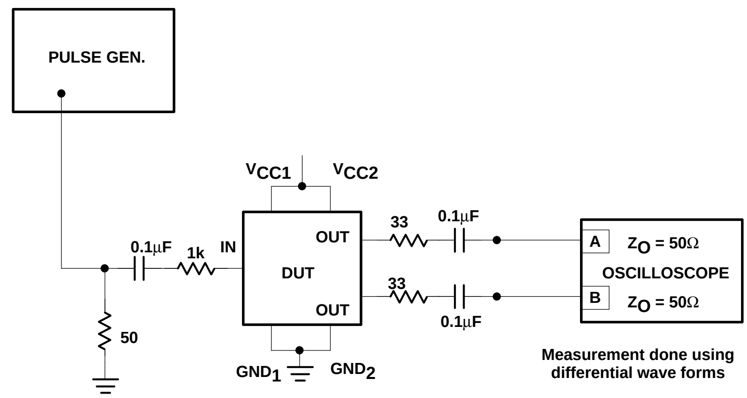
TEST CIRCUITS (Continued)

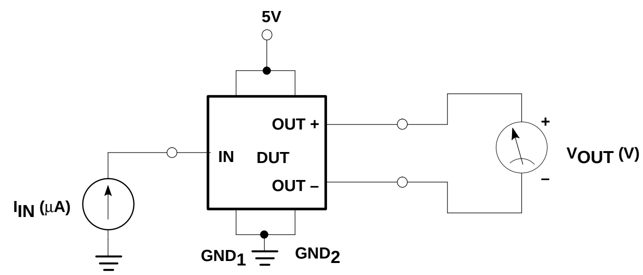


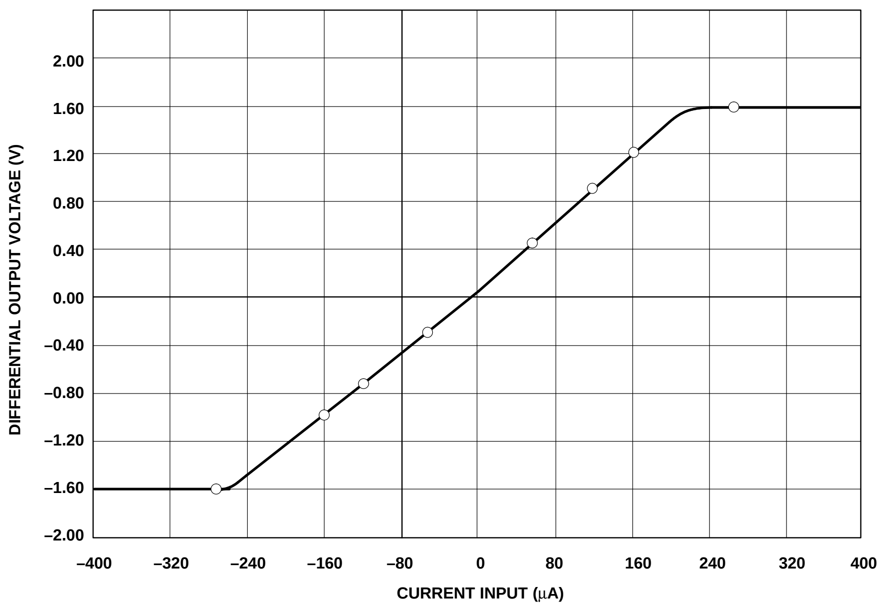
Test Circuit 7

SD00322

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5210 TEST CONDITIONS

Procedure 1

R_T measured at 60µA

$R_T = (V_{O1} - V_{O2})/(+60\mu A - (-60\mu A))$

Where: V_{O1} Measured at I_{IN} = +60µA

V_{O2} Measured at I_{IN} = –60µA

Procedure 2

Linearity = 1 – ABS($(V_{OA} - V_{OB})$ / $(V_{O3} - V_{O4})$)

Where: V_{O3} Measured at I_{IN} = +120µA

V_{O4} Measured at I_{IN} = –120µA

$V_{OA} = R_T \cdot (+\ 120\mu A) + V_{OB}$

$V_{OB} = R_T \cdot (-\ 120\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$

Where: V_{O7} Measured at I_{IN} = +260µA

V_{O8} Measured at I_{IN} = –260µA

Procedure 4

I_{IN} Test Pass Conditions:

$V_{O7} - V_{O5}$ > 20mV and $V_{06} - V_{O5}$ > 20mV

Where: V_{O5} Measured at I_{IN} = +160µA

V_{O6} Measured at I_{IN} = –160µA

V_{O7} Measured at I_{IN} = +260µA

V_{O8} Measured at I_{IN} = –260µA

Test Circuit 8

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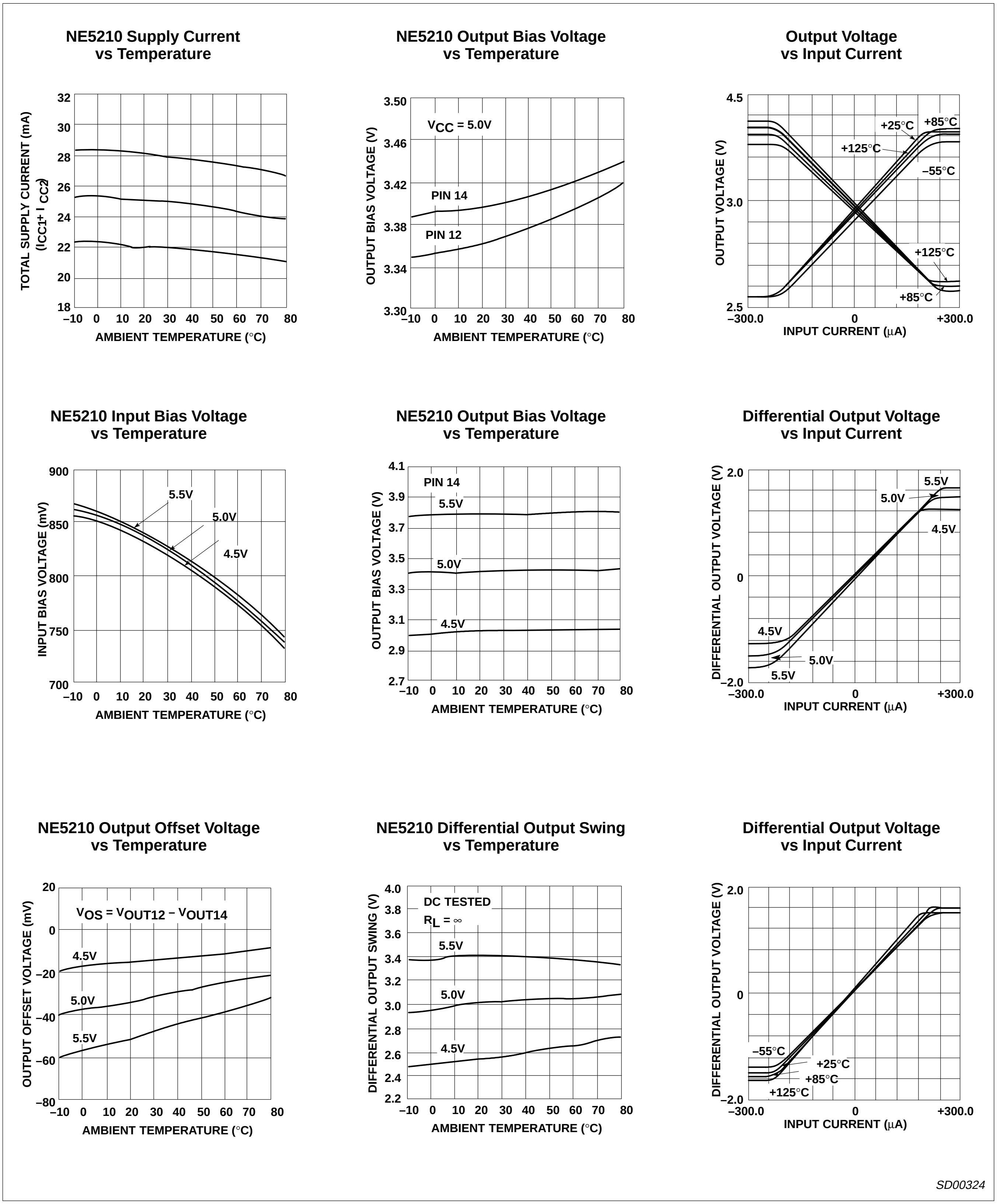
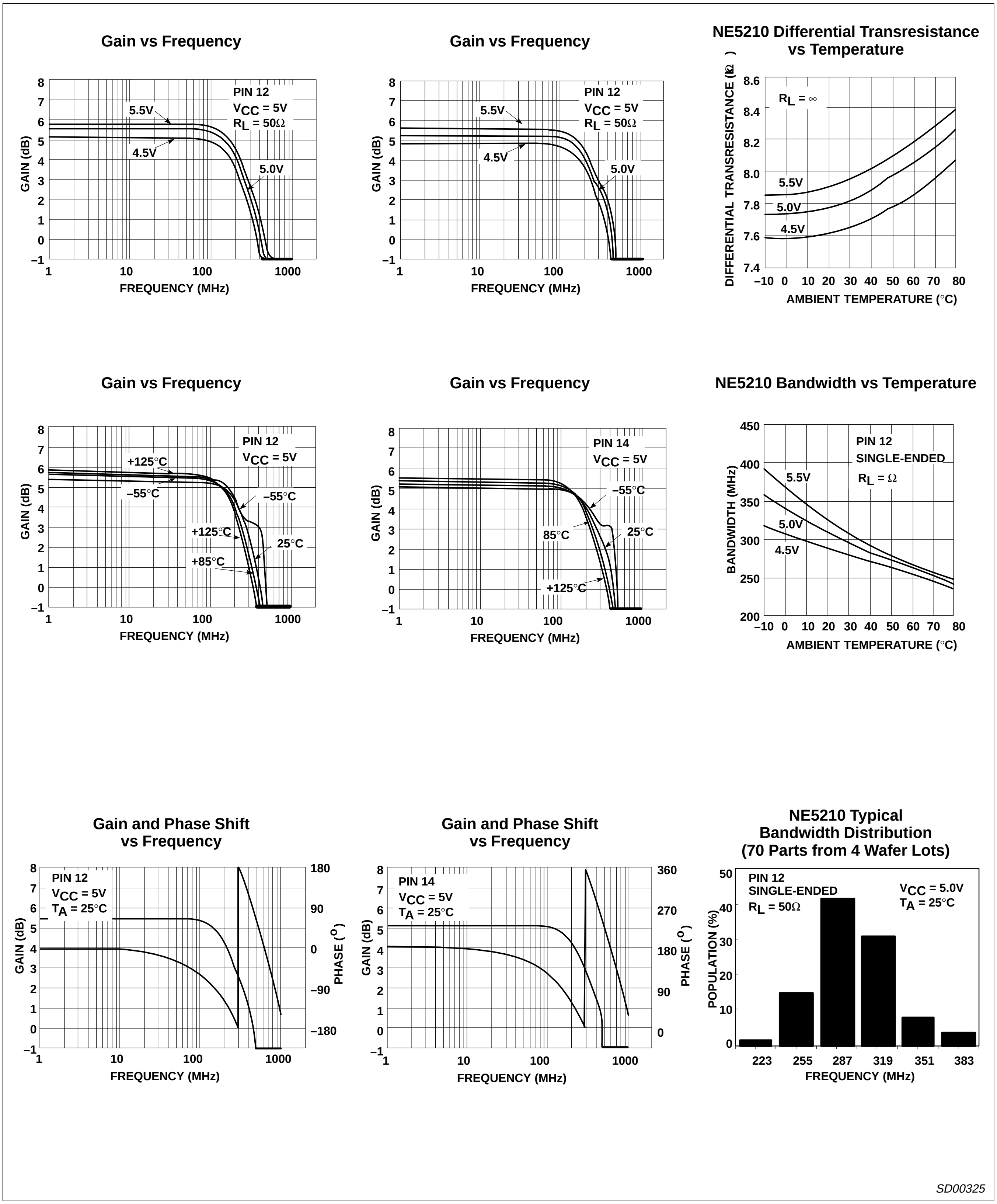
TYPICAL PERFORMANCE CHARACTERISTICS

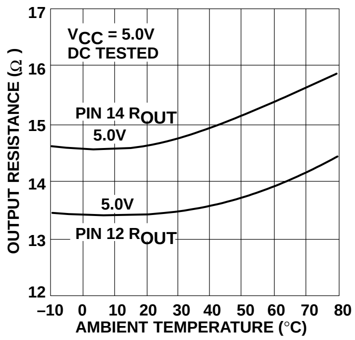


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

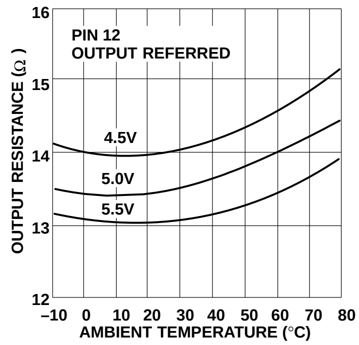


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

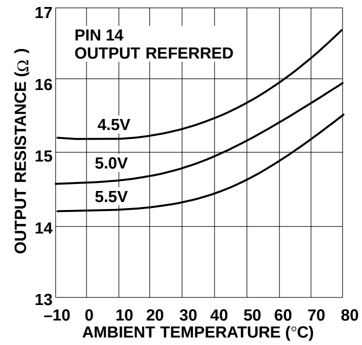
NE5210 Output Resistance vs Temperature



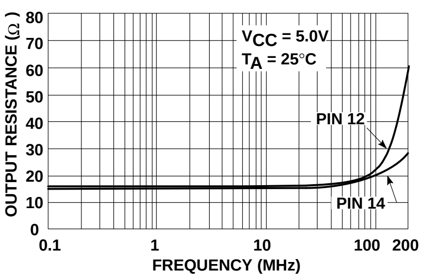
NE5210 Output Resistance vs Temperature



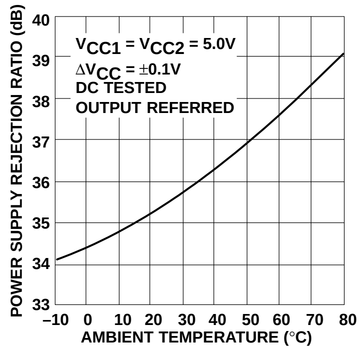
NE5210 Output Resistance vs Temperature



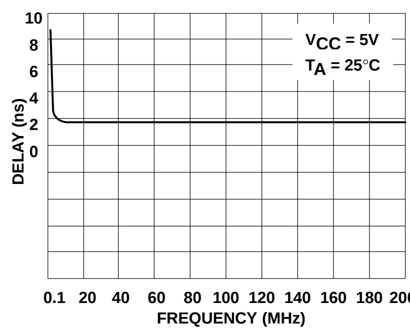
Output Resistance vs Frequency



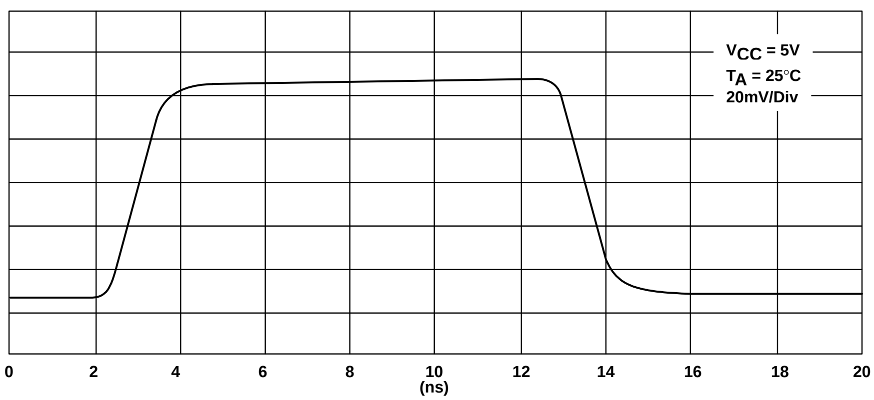
NE5210 Power Supply Rejection Ratio vs Temperature



Group Delay



Output Step Response



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THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240µA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15} – Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11} – Q_{12} which are biased by constant current sources. The collectors of Q_{11} – Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

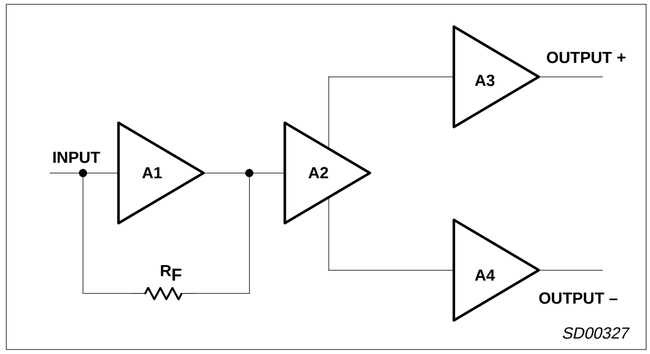


Figure 1. NE5210 – Block Diagram

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in
parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3.6K}{71} = 51$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2 \quad R_{IN} \; C_{IN}}$$

Assuming typical values for R_F = 3.6kΩ, R_{IN} = 60Ω, C_{IN} = 7.5pF

$$f_{-3dB} = \frac{1}{2 \quad 7.5pF \; 60} = 354MHz$$

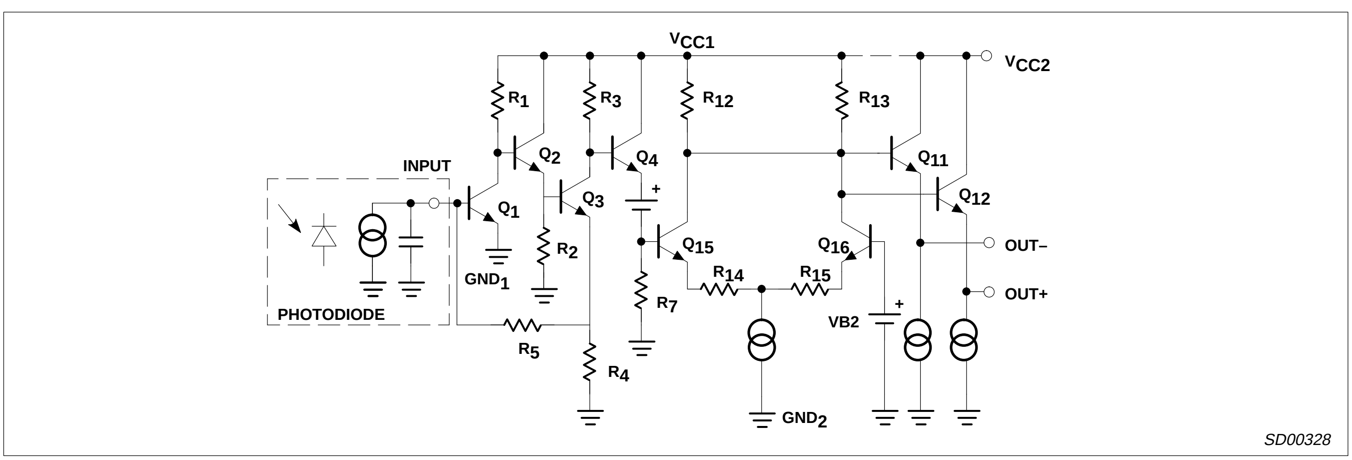


Figure 2. Transimpedance Amplifier

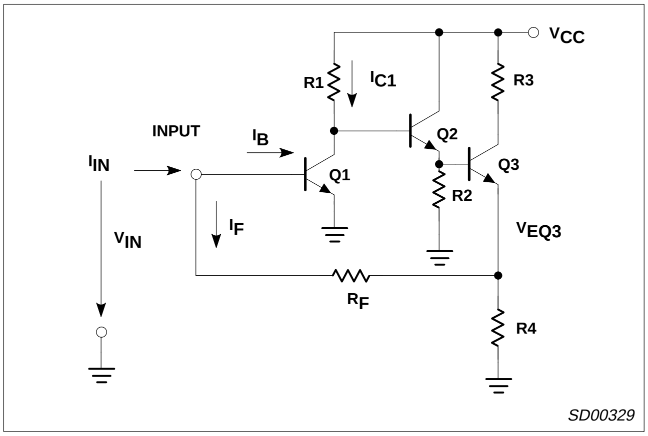


Figure 3. Shunt-Series Input Stage

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA$_{RMS}$ in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240µA and a wideband noise of I_{EQ}=66nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = 20\log\frac{(\text{Max. input current})\ (\text{PK})}{(\text{Peak noise current})\ (\text{RMS})\cdot\sqrt{2}}$$

$$= 20\log\frac{(240\cdot10^{-6})}{(\sqrt{2}\ 66\ 10^{-9})} = 68\text{dB}$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ; (meters)
Energy of one Photon = $\frac{hc}{\ }$ watt sec (Joule)

Where h=Planck's Constant = 6.6 × 10^{-34} Joule sec.
c = speed of light = 3 × 10^8 m/sec
c / λ = optical frequency (Hz)
No. of incident photons/sec= where P=optical incident power

$$\text{No. of incident photons/sec} = \frac{P}{hs}$$

where P = optical incident power

$$\text{No. of generated electrons/sec} = \ .\ \frac{P}{hs}$$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$I = \ .\ \frac{P}{hs}\cdot e\ \text{Amps (Coulombs sec.)}$$

where e = electron charge = 1.6 × 10^{-19} Coulombs

$$\text{Responsivity R} = \frac{\cdot e}{hs}\text{Amp/watt}$$

$$I = P\cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66\cdot10^{-9}}{(1.6\cdot10^{-19})(200\cdot10^{6})} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\ }B\ Z = 12\ 2.3\cdot10^{-19}$$

$$200\cdot10^{6}\ 2063$$

$$= 1139\text{nW} = -29.4\text{dBm}$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\ }{hc}$$

$$= \frac{1139\cdot10^{-9}\cdot1.6\cdot10^{-19}}{2.3\cdot10^{-19}}$$

$$= 792\text{nA}$$

Choosing the maximum peak overload current of I_{avMAX}=240µA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{q} = \frac{2.3\cdot10^{-19}}{1.6\cdot10^{-19}}240\cdot10^{-6}$$

Thus the optical dynamic range, D_O is:

D_O = P_{avMAX} - P_{avMIN} = -4.6 -(-29.4) = 24.8dB.

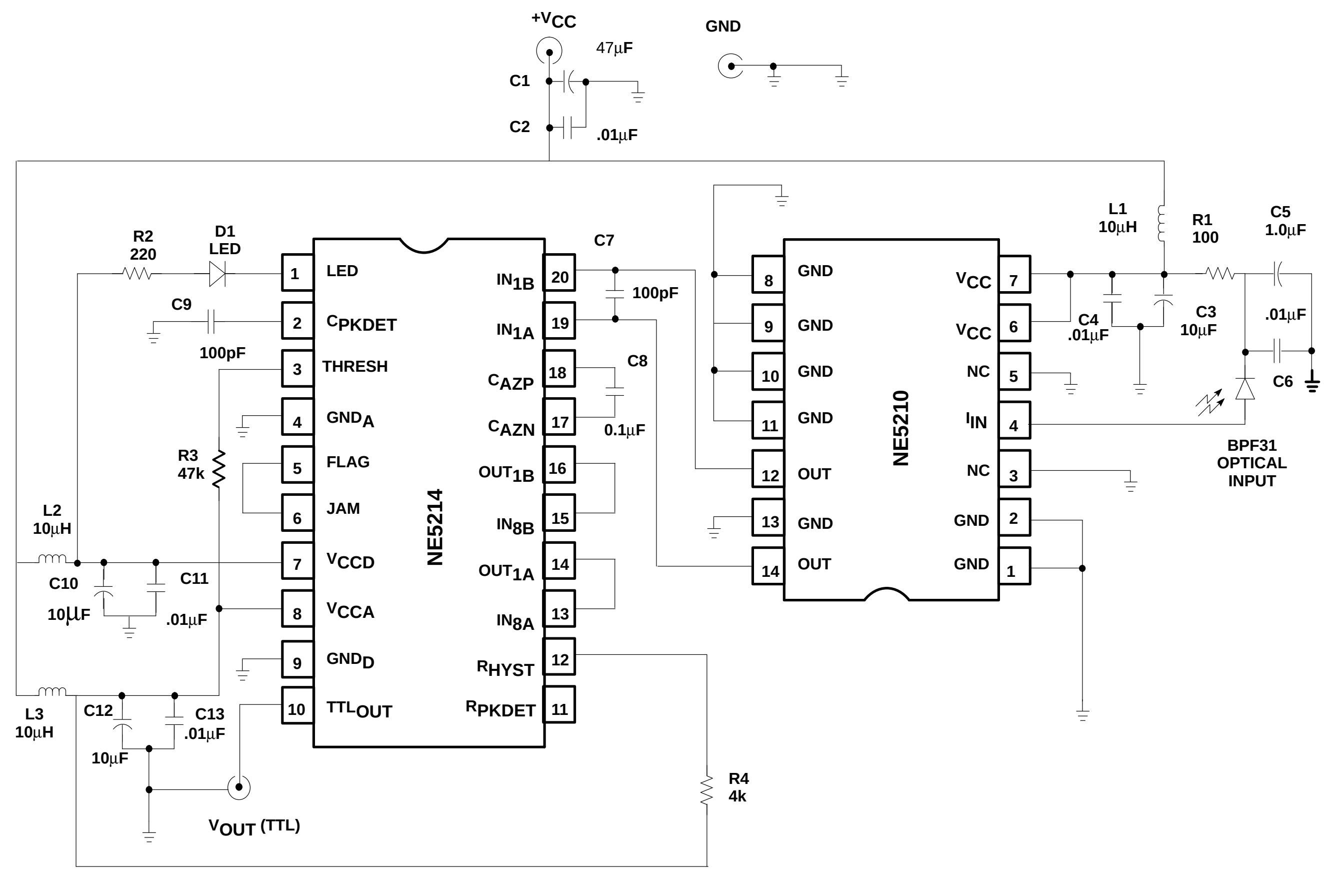
This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ
The capacitor C7 decreases the NE5210 bandwidth to improve overall S/N ratio in the DC–50MHz band, but does create extra high frequency noise on the NE5210 V_{CC} pin(s).

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Figure 4. A 50Mb/s Fiber Optic Receiver

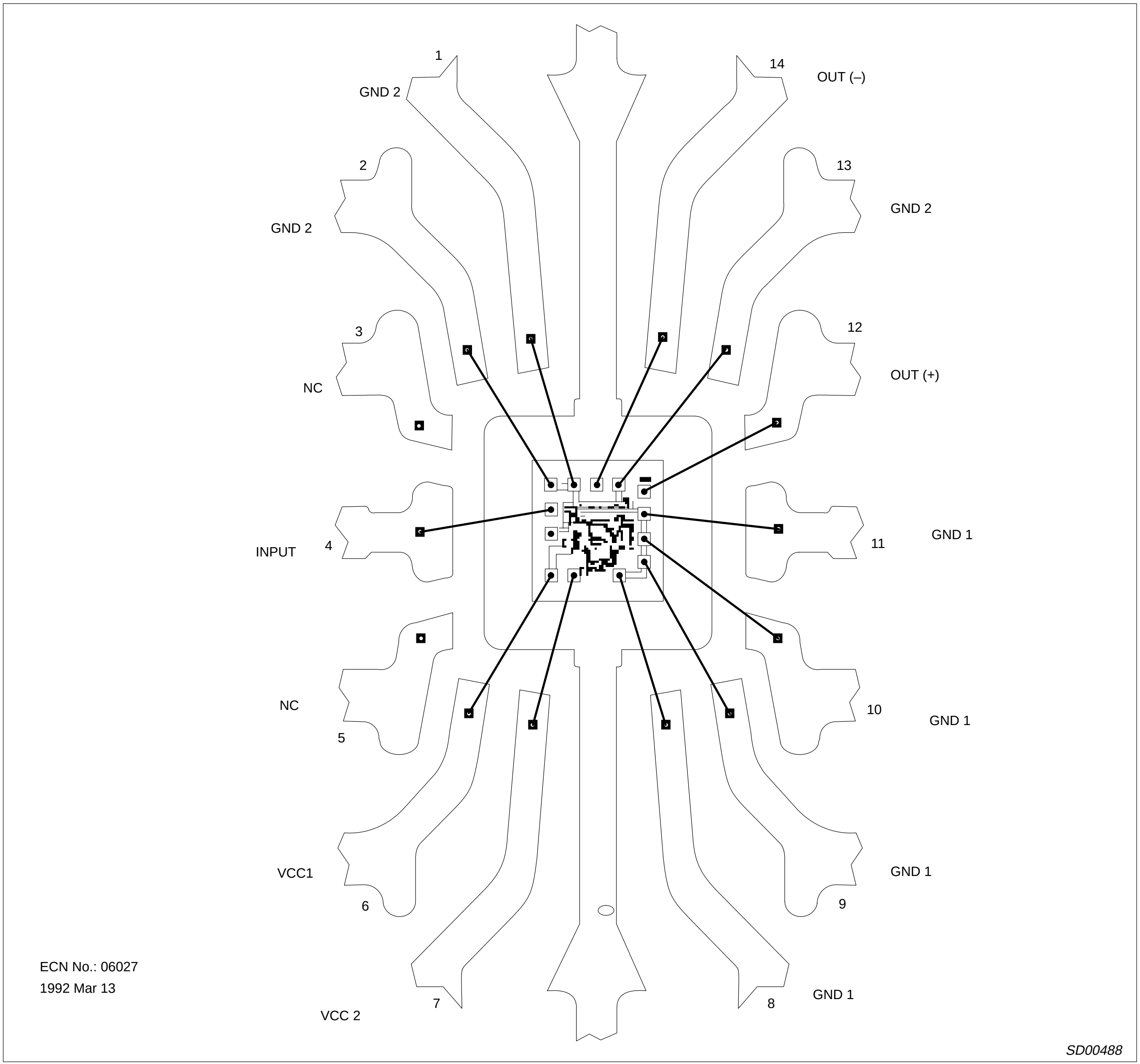

Figure 5. NE5210 Bonding Diagram

Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.